ANALOG DEVICES

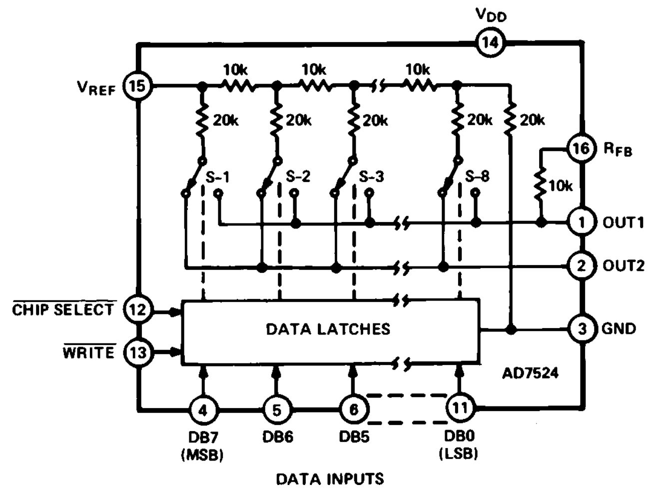
CMOS 8-Bit Buffered Multiplying DAC

AD7524

FEATURES
- Microprocessor Compatible (6800, 8085, Z80, Etc.)
- TTL/CMOS Compatible Inputs
- On-Chip Data Latches
- Endpoint Linearity
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)
- Latch Free (No Protection Schottky Required)

APPLICATIONS
- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits
- Bus Structured Instruments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7524 is a low cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

Basically an 8-bit DAC with input latches, the AD7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the AD7524 provides accuracy to 1/8 LSB with a typical power dissipation of less than 10 milliwatts.

A newly improved design eliminates the protection Schottky previously required and guarantees TTL compatibility when using a +5 V supply. Loading speed has been increased for compatibility with most microprocessors.

Featuring operation from +5 V to +15 V, the AD7524 interfaces directly to most microprocessor buses or output ports.

Excellent multiplying characteristics (2- or 4-quadrant) make the AD7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

ORDERING GUIDE

Model[1]	Temperature Range	Nonlinearity (V_{DD} = +15 V)	Package Option[2]
AD7524JN	–40°C to +85°C	±1/2 LSB	N-16
AD7524KN	–40°C to +85°C	±1/4 LSB	N-16
AD7524LN	–40°C to +85°C	±1/8 LSB	N-16
AD7524JP	–40°C to +85°C	±1/2 LSB	P-20A
AD7524KP	–40°C to +85°C	±1/4 LSB	P-20A
AD7524LP	–40°C to +85°C	±1/8 LSB	P-20A
AD7524JR	–40°C to +85°C	±1/2 LSB	R-16A
AD7524AQ	–40°C to +85°C	±1/2 LSB	Q-16
AD7524BQ	–40°C to +85°C	±1/4 LSB	Q-16
AD7524CQ	–40°C to +85°C	±1/8 LSB	Q-16
AD7524SQ	–55°C to +125°C	±1/2 LSB	Q-16
AD7524TQ	–55°C to +125°C	±1/4 LSB	Q-16
AD7524UQ	–55°C to +125°C	±1/8 LSB	Q-16
AD7524SE	–55°C to +125°C	±1/2 LSB	E-20A
AD7524TE	–55°C to +125°C	±1/4 LSB	E-20A
AD7524UE	–55°C to +125°C	±1/8 LSB	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC drawing #5962-87700.
[2]E = Leadless Ceramic Chip Carrier: N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD7524–SPECIFICATIONS (V_{REF} = +10 V, V_{OUT1} = V_{OUT2} = 0 V, unless otherwise noted)

Parameter	Limit, T_A = +25°C V_{DD} = +5 V	V_{DD} = +15 V	Limit, T_{MIN}, T_{MAX}[1] V_{DD} = 5 V	V_{DD} = +15 V	Units	Test Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Relative Accuracy						
J, A, S Versions	±1/2	±1/2	±1/2	±1/2	LSB max	
K, B, T Versions	±1/2	±1/4	±1/2	±1/4	LSB max	
L, C, U Versions	±1/2	±1/8	±1/2	±1/8	LSB max	
Monotonicity	Guaranteed	Guaranteed	Guaranteed	Guaranteed		
Gain Error[2]	±2 1/2	±1 1/4	±3 1/2	±1 1/2	LSB max	
Average Gain TC[3]	±40	±10	±40	±10	ppm/°C	Gain TC Measured from +25°C to T_{MIN} or from +25°C to T_{MAX}
DC Supply Rejection,[3] $\Delta Gain/\Delta V_{DD}$	0.08	0.02	0.16	0.04	% FSR/% max	ΔV_{DD} = ±10%
	0.002	0.001	0.01	0.005	% FSR/% typ	
Output Leakage Current						
I_{OUT1} (Pin 1)	±50	±50	±400	±200	nA max	DB0–DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V; V_{REF} = ±10 V
I_{OUT2} (Pin 2)	±50	±50	±400	±200	nA max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0 V; V_{REF} = ±10 V
DYNAMIC PERFORMANCE						
Output Current Settling Time[3] (to 1/2 LSB)	400	250	500	350	ns max	OUT1 Load = 100 Ω, C_{EXT} = 13 pF; $\overline{WR}$, $\overline{CS}$ = 0 V; DB0–DB7 = 0 V to V_{DD} to 0 V.
AC Feedthrough[3]						
at OUT1	0.25	0.25	0.5	0.5	% FSR max	V_{REF} = ±10 V, 100 kHz Sine Wave; DB0–DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V
at OUT2	0.25	0.25	0.5	0.5	% FSR max	
REFERENCE INPUT						
R_{IN} (Pin 15 to GND)[4]	5	5	5	5	kΩ min	
	20	20	20	20	kΩ max	
ANALOG OUTPUTS						
Output Capacitance[3]						
C_{OUT1} (Pin 1)	120	120	120	120	pF max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0 V
C_{OUT2} (Pin 2)	30	30	30	30	pF max	
C_{OUT1} (Pin 1)	30	30	30	30	pF max	DB0–DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V
C_{OUT2} (Pin 2)	120	120	120	120	pF max	
DIGITAL INPUTS						
Input HIGH Voltage Requirement V_{IH}	+2.4	+13.5	+2.4	+13.5	V min	
Input LOW Voltage Requirement V_{IL}	+0.8	+1.5	+0.5	+1.5	V max	
Input Current I_{IN}	±1	±1	±10	±10	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]						
DB0–DB7	5	5	5	5	pF max	V_{IN} = 0 V
$\overline{WR}$, $\overline{CS}$	20	20	20	20	pF max	V_{IN} = 0 V
SWITCHING CHARACTERISTICS						
Chip Select to Write Setup Time[5]						See Timing Diagram
t_{CS}						t_{WR} = t_{CS}
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Chip Select to Write Hold Time						
t_{CH}						
All Grades	0	0	0	0	ns min	
Write Pulse Width						
t_{WR}						$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Data Setup Time						
t_{DS}						
AD7524J, K, L, A, B, C	135	60	170	80	ns min	
AD7524S, T, U	135	60	170	100	ns min	
Data Hold Time						
t_{DH}						
All Grades	10	10	10	10	ns min	
POWER SUPPLY						
I_{DD}	1	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	100	100	500	500	µA max	All Digital Inputs 0 V or V_{DD}

NOTES

[1]Temperature ranges as follows: J, K, L versions: –40°C to +85°C
A, B, C versions: –40°C to +85°C
S, T, U versions: –55°C to +125°C

[2]Gain error is measured using internal feedback resistor. Full-Scale Range (FSR) = V_{REF}.

[3]Guaranteed not tested.

[4]DAC thin-film resistor temperature coefficient is approximately –300 ppm/°C.

[5]AC parameter, sample tested @ +25°C to ensure conformance to specification.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C, unless otherwise noted)

V_{DD} to GND . . . . –0.3 V, +17 V
V_{RFB} to GND . . . . ±25 V
V_{REF} to GND . . . . ±25 V
Digital Input Voltage to GND . . . . –0.3 V to V_{DD} +0.3 V
OUT1, OUT2 to GND . . . . –0.3 V to V_{DD} +0.3 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Power Dissipation (Any Package)
To +75°C . . . . 450 mW
Derates above 75°C by . . . . 6 mW/°C
Operating Temperature
Commercial (J, K, L) . . . . –40°C to +85°C
Industrial (A, B, C) . . . . –40°C to +85°C
Extended (S, T, U) . . . . –55°C to +125°C
Storage Temperature . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . +300°C

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7524 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TERMINOLOGY

RELATIVE ACCURACY: A measure of the deviation from a straight line through the end points of the DAC transfer function. Normally expressed as a percentage of full scale range. For the AD7524 DAC, this holds true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

GAIN ERROR: Gain Error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in LSBs. Gain Error is adjustable to zero with an external potentiometer.

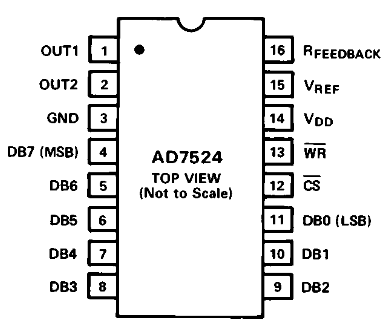
FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from OUT1 and OUT2 terminals to ground.

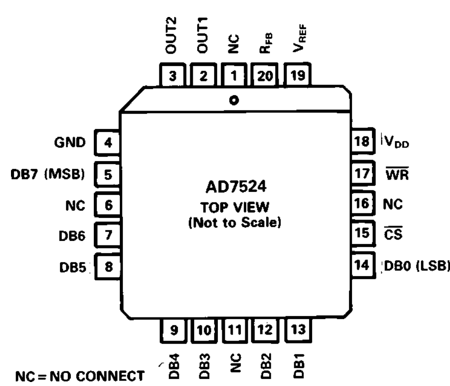
OUTPUT LEAKAGE CURRENT: Current which appears on OUT1 terminal with all digital inputs LOW or on OUT2 terminal when all inputs are HIGH. This is an error current which contributes an offset voltage at the amplifier output.

PIN CONFIGURATIONS

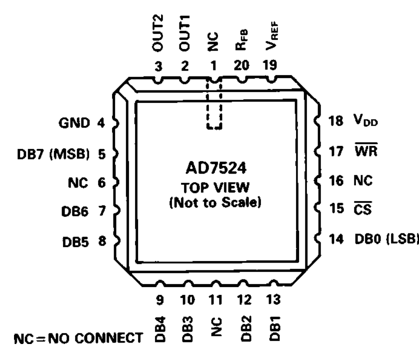
DIP, SOIC



PLCC



LCCC



CIRCUIT DESCRIPTION

CIRCUIT INFORMATION

The AD7524, an 8-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and eight N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

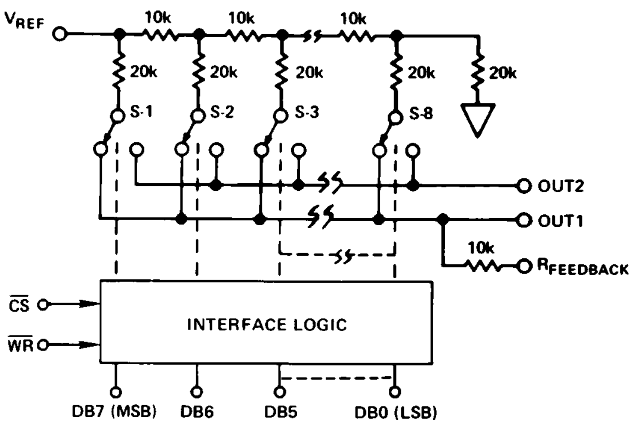


Figure 1. Functional Diagram

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuit for all digital inputs LOW is shown in Figures 2. In Figure 2 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{1}{256}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switches is 120 pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 30 pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs high is similar to Figure 2 however, the "ON" switches are now on terminal OUT1, hence the 120 pF appears at that terminal.

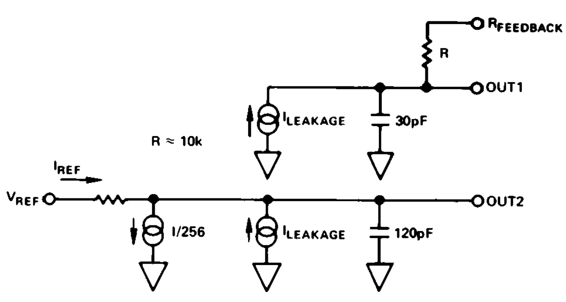


Figure 2. AD7524 DAC Equivalent Circuit—All Digital Inputs Low

INTERFACE LOGIC INFORMATION

MODE SELECTION

AD7524 mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

WRITE MODE

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the AD7524 is in the WRITE mode, and the AD7524 analog output responds to data activity at the DB0–DB7 data bus inputs. In this mode, the AD7524 acts like a nonlatched input D/A converter.

HOLD MODE

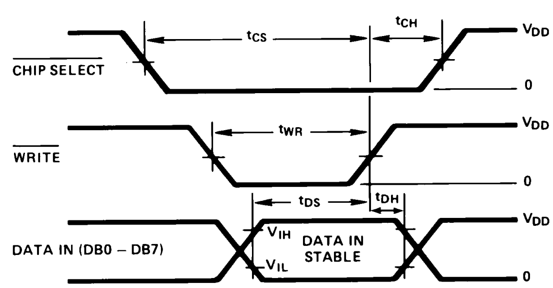
When either $\overline{CS}$ or $\overline{WR}$ is HIGH, the AD7524 is in the HOLD mode. The AD7524 analog output holds the value corresponding to the last digital input present at DB0–DB7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the HIGH state.

MODE SELECTION TABLE

$\overline{CS}$	$\overline{WR}$	Mode	DAC Response
L	L	Write	DAC responds to data bus (DB0–DB7) inputs.
H	X	Hold	Data bus (DB0–DB7) is Locked Out:
X	H	Hold	DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed HIGH state.

L = Low State, H = High State, X = Don't Care.

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. All input signal rise and fall times measured from 10% to 90% of V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. Timing Measurement Reference level is $\frac{V_{IH} + V_{IL}}{2}$
3. $t_{DS} + t_{DH}$ is approximately constant at 145ns min at +25°C, V_{DD} = +5V and t_{wr} = 170ns min. The AD7524 is specified for a minimum t_{DH} of 10ns, however, in applications where t_{DH} > 10ns, t_{DS} may be reduced accordingly up to the limit t_{DS} = 65ns, t_{DH} = 80ns.

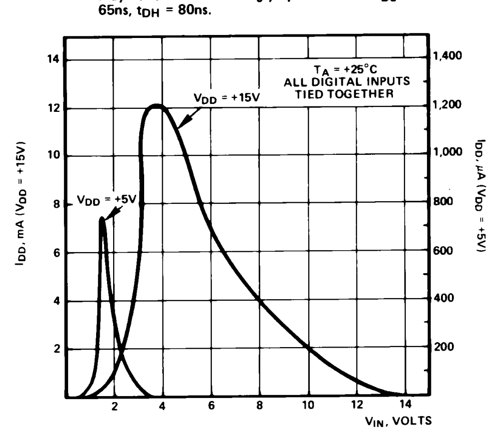


Figure 3. Supply Current vs. Logic Level

Typical plots of supply current, I_{DD}, versus logic input voltage, V_{IN}, for V_{DD} = +5 V and V_{DD} = +15 V are shown above.

ANALOG CIRCUIT CONNECTIONS

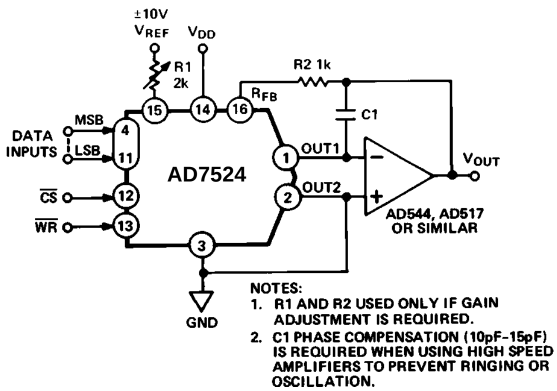


Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

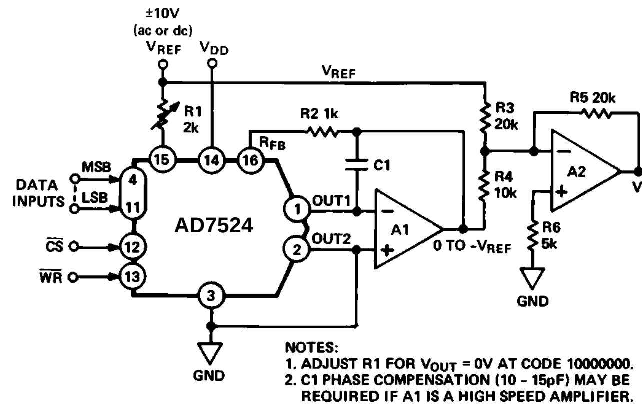


Figure 5. Bipolar (4-Quadrant) Operation

Table I. Unipolar Binary Code Table

Digital Input MSB LSB	Analog Output
1111 1111	$-V_{REF}$ (255/256)
1000 0001	$-V_{REF}$ (129/256)
1000 0000	$-V_{REF}$ (128/256) = $-V_{REF}/2$
0111 1111	$-V_{REF}$ (127/256)
0000 0001	$-V_{REF}$ (1/256)
0000 0000	$-V_{REF}$ (0/256) = 0

Note: 1 LSB = $(2^{-8})(V_{REF})$ = 1/256 (V_{REF})

Table II. Bipolar (Offset Binary) Code Table

Digital Input MSB LSB	Analog Output
1111 1111	$+V_{REF}$ (127/128)
1000 0001	$+V_{REF}$ (1/128)
1000 0000	0
0111 1111	$-V_{REF}$ (1/128)
0000 0001	$-V_{REF}$ (127/128)
0000 0000	$-V_{REF}$ (128/128)

Note: 1 LSB = $(2^{-7})(V_{REF})$ = 1/128 (V_{REF})

MICROPROCESSOR INTERFACE

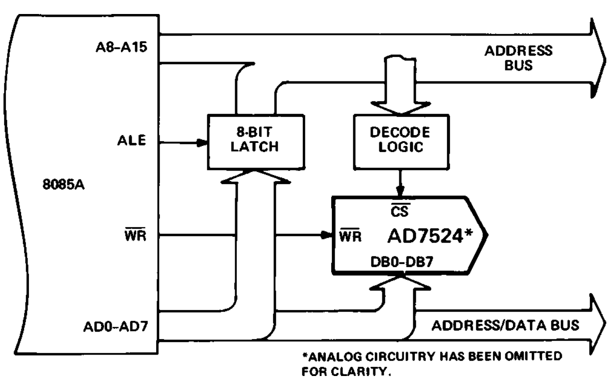


Figure 6. AD7524/8085A Interface

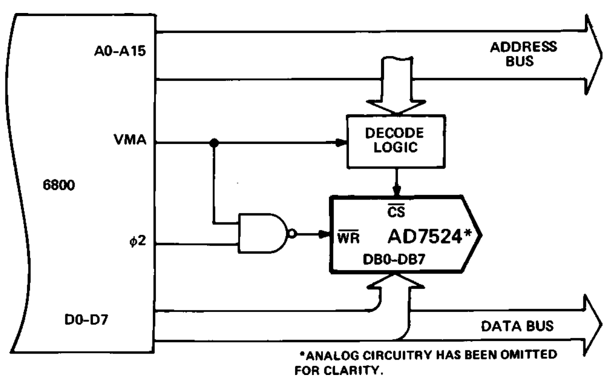


Figure 7. AD7524/MC6800 Interface

POWER GENERATION

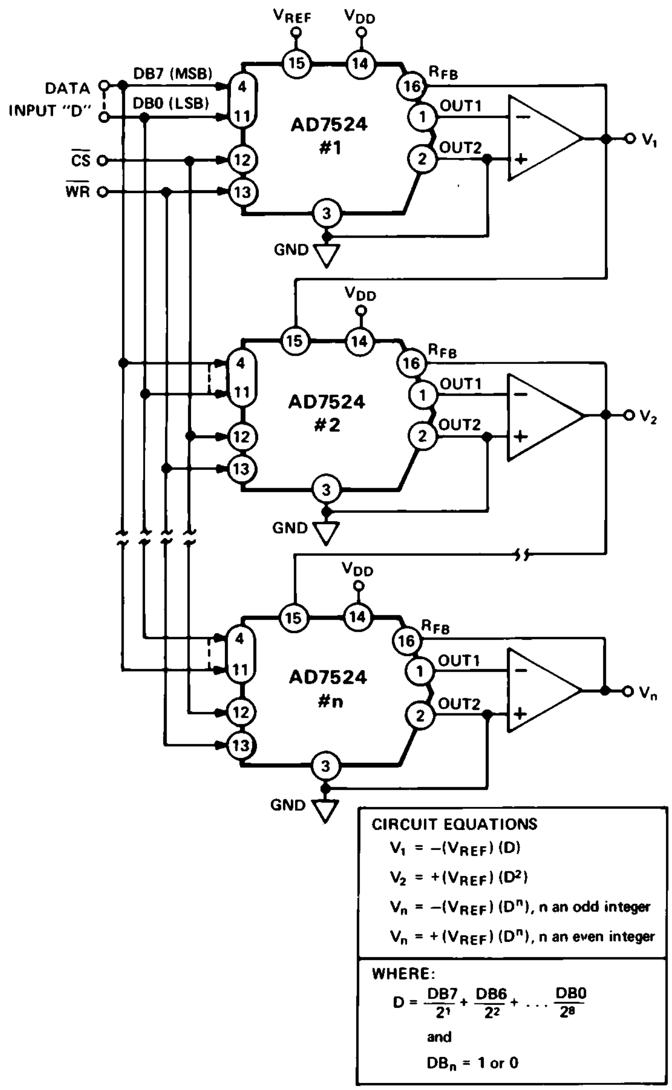
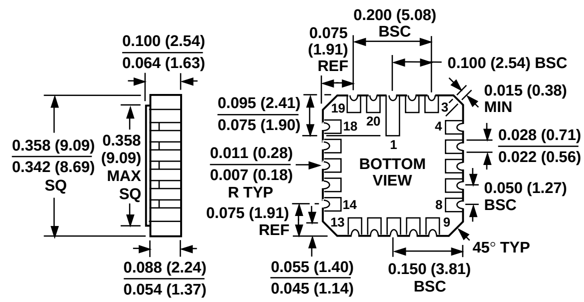


Figure 8.

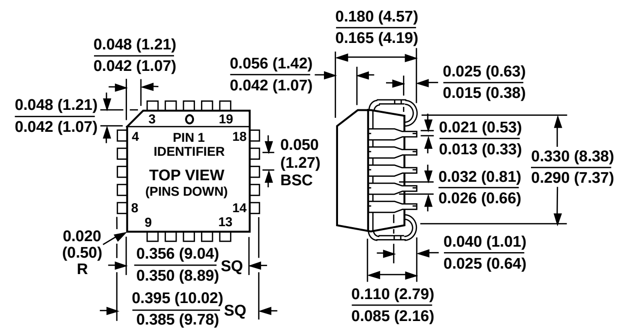
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

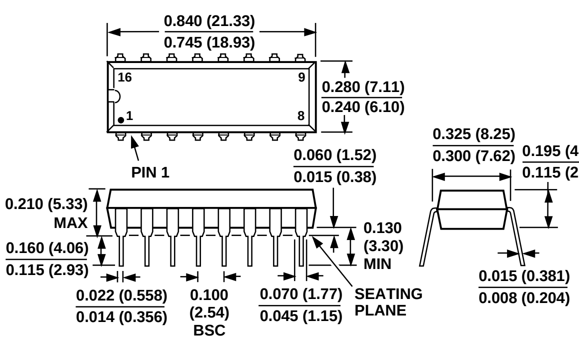
20-Terminal Ceramic Leadless Chip Carrier (E-20A)



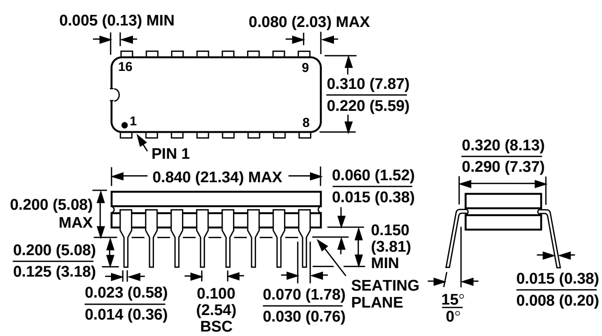
20-Lead Plastic Leadless Chip Carrier (PLCC) (P-20A)



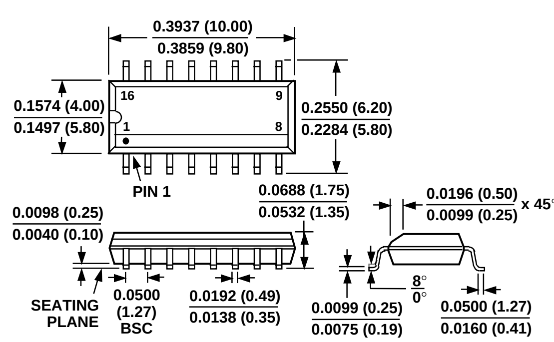
16-Lead Plastic DIP (Narrow) (N-16)



16-Lead Cerdip (Q-16)



16-Lead Narrow-Body (SOIC) (R-16A)



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